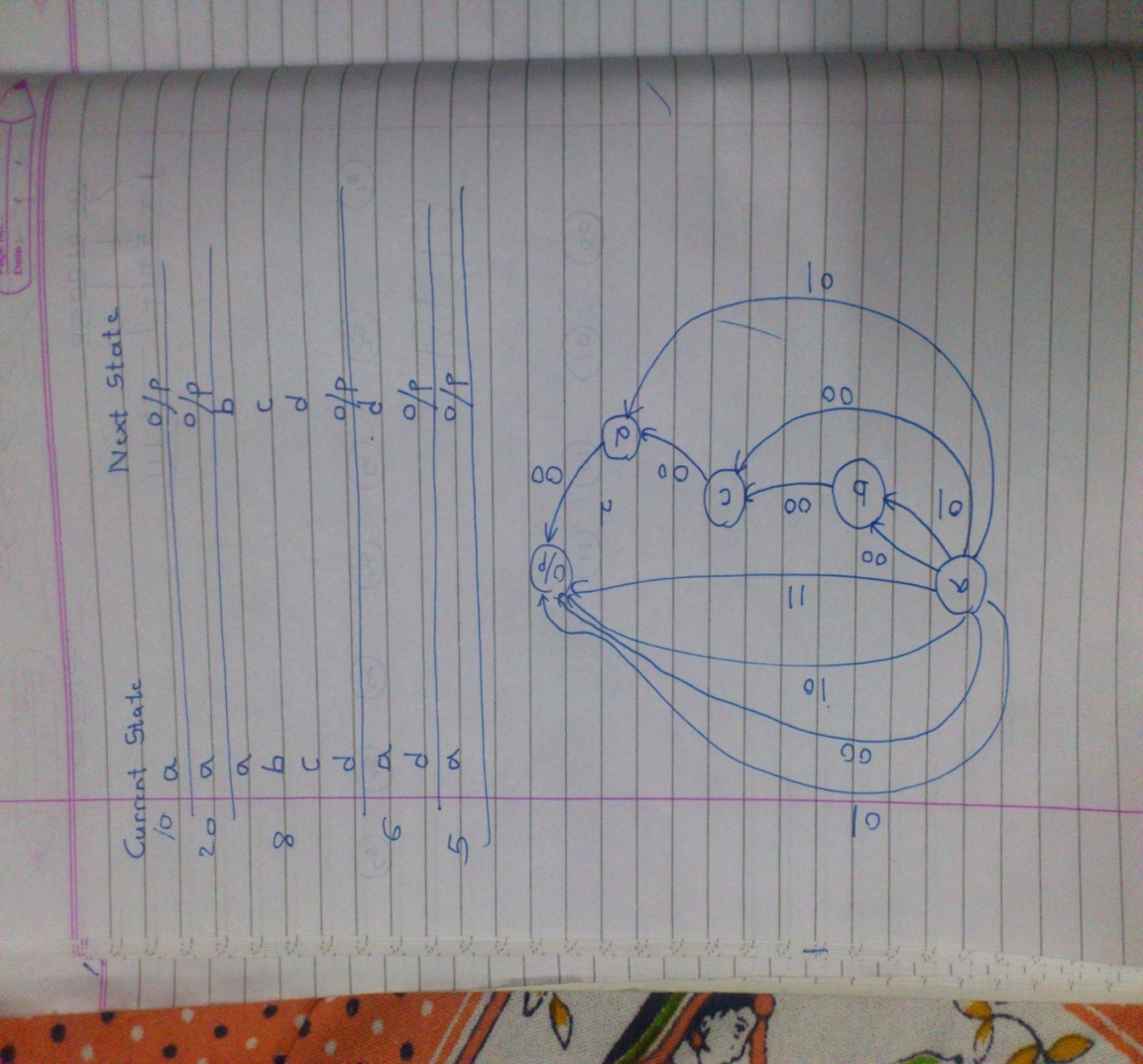
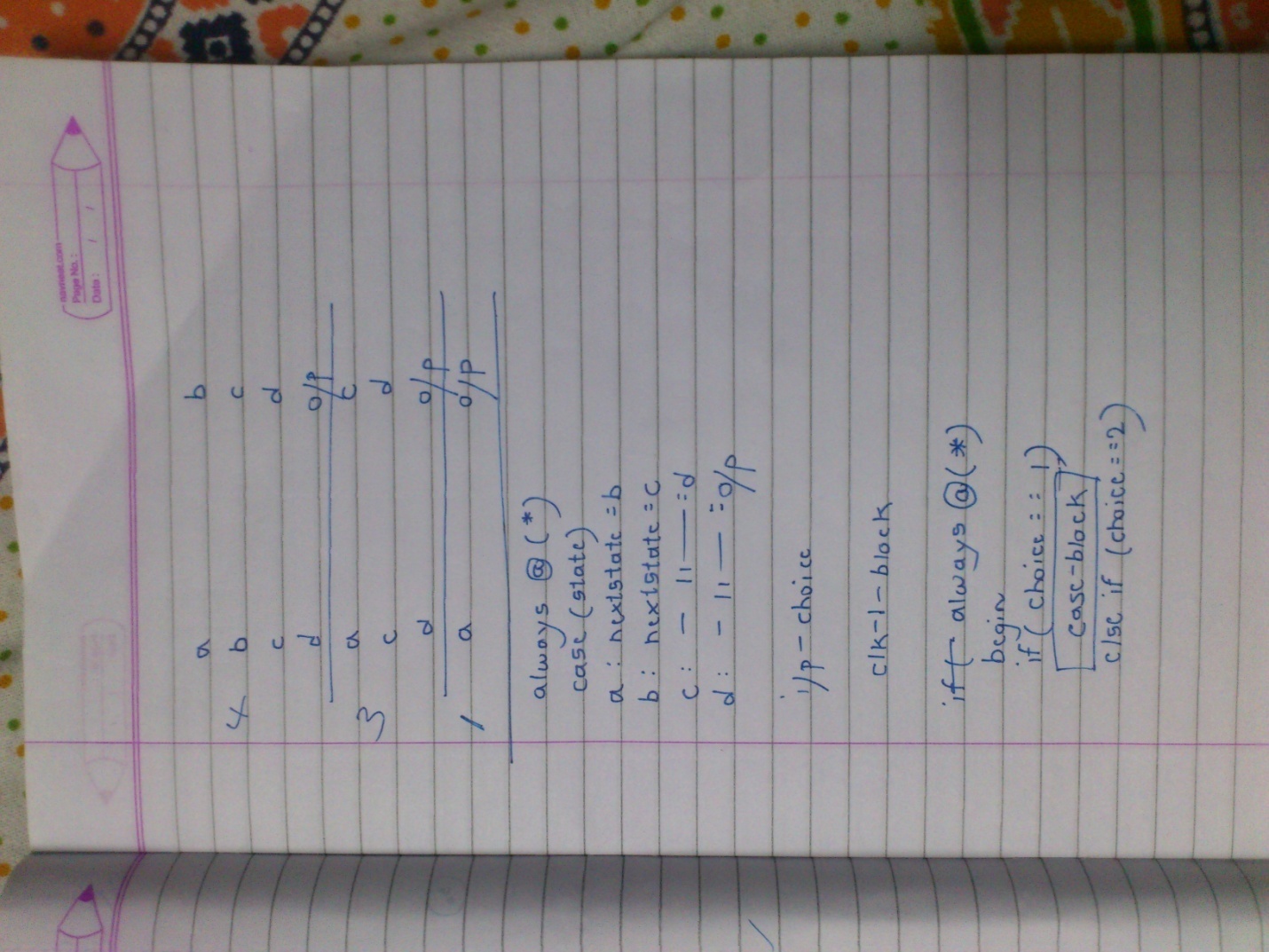
Vending Machine

Understanding the problem:

* Our goal is to design a vending machine which would return an ice-cream flavor as per the customer’s choice from the given 8 flavors.
* Restriction provided is that customer has only four denominations of money: $1, $5, $10, $20.
* So, generated hardware would be a ‘Finite State Machine’ .

Devising the plan:





* Before drawing the state diagram, we have suitably assumed that the customer would pay for the flavor in minimum possible combinations of given money denominations.
* For example, if the customer wants to buy ‘chocolate chips’ of $10,he would enter a $10 coin and not two $5 coins or other possible chances.
* As seen in the state diagram, we have 4 distinct states and 1 theoretical output state as maximum transitions possible are 4.
* According to the choice, state transitions will occur from state ‘a’ to ‘o/p’ state.
* These transitions would be unique for each choice.
* We have 5 states. Hence flipflops used must be 3.

|  |  |  |
| --- | --- | --- |
| Flavour | Combination of money | Choice |
| Banana Strawberries | 1 | 000 |
| Black Walnut | 1+1+1 | 001 |
| Rum Raisin | 1+1+1+1 | 010 |
| Caramel Praline Cheesecake | 5 | 011 |
| Chocolate Moose | 5+1 | 100 |
| Super Fudge Truffle | 5+1+1+1 | 101 |
| Chocolate Chips | 10 | 110 |
| Very Berry Strawberry | 20 | 111 |

* For example- for Super Fudge Truffle($8) there are four coins entered 5,1,1,1. Hence four transitions will take place a to b, b to c, c to d, d to op.

Carrying out the plan:

**Verilog code:**

module VM1(

input [2:0] choice,

output [2:0]y,

input clk,

input reset

);

reg[2:0] state,nextstate;

parameter a=3'b000;

parameter b=3'b001;

parameter c=3'b010;

parameter d=3'b011;

parameter op=3'b100;

always @ (posedge clk,posedge reset)

begin

if (reset) state<=a;

else state<= nextstate;

end

always @ (\*)

if(choice==3'b000)

begin

case(state)

a: nextstate=op;

default: nextstate=a;

endcase

end

else if(choice==3'b001)

begin

case(state)

a: nextstate=c;

c: nextstate=d;

d: nextstate=op;

default: nextstate=a;

endcase

end

else if(choice==3'b010)

begin

case(state)

a: nextstate=b;

b: nextstate=c;

c: nextstate=d;

d: nextstate=op;

default: nextstate=a;

endcase

end

else if(choice==3'b011)

begin

case(state)

a: nextstate=op;

default: nextstate=a;

endcase

end

else if(choice==3'b100)

begin

case(state)

a: nextstate=d;

d: nextstate=op;

default: nextstate=a;

endcase

end

else if(choice==3'b101)

begin

case(state)

a: nextstate=b;

b: nextstate=c;

c: nextstate=d;

d: nextstate=op;

default: nextstate=a;

endcase

end

else if(choice==3'b110)

begin

case(state)

a: nextstate=op;

default: nextstate=a;

endcase

end

else if(choice==3'b111)

begin

case(state)

a: nextstate=op;

default: nextstate=a;

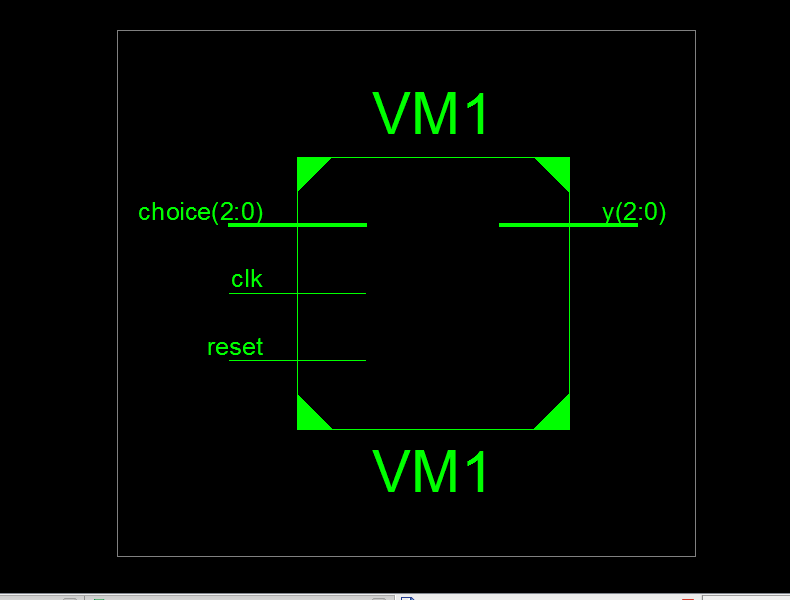
endcase

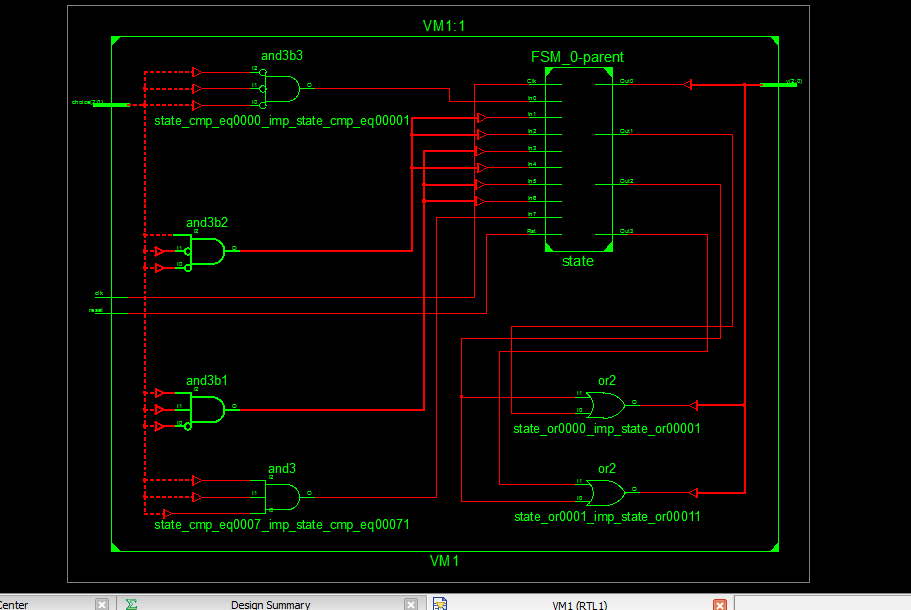
end

else nextstate=a;

assign y=state;

endmodule

**RTL Schematic:**

****

**Test Bench:**

modulefinal\_tb;

// Inputs

reg [2:0] choice;

regclk;

reg reset;

// Outputs

wire [2:0] y;

// Instantiate the Unit Under Test (UUT)

VM1 uut (

.choice(choice),

.y(y),

.clk(clk),

.reset(reset)

);

initial begin

// Initialize Inputs

choice = 0;

clk = 0;

reset = 0;

// Wait 100 ns for global reset to finish

#100;

// Add stimulus here

#100;

choice=3'b001;

clk=1'b1;

#10;

clk=1'b0;

#10;

clk=1'b1;

#10;

clk=1'b0;

#10;

clk=1'b1;

#10;

clk=1'b0;

#10;

clk=1'b1;

#10;

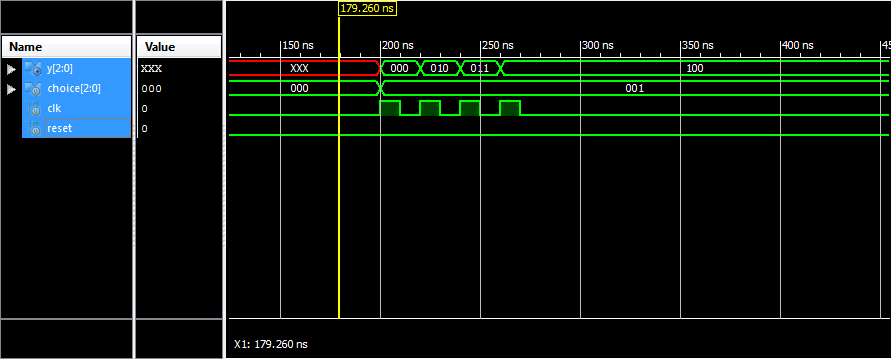
clk=1'b0;

#10;

end

endmodule

**Output:**

****

Looking Back:

* We can see that at every positive edge of the clock, state transition occurs.
* For each choice, number of clock pulses required to reach at the output state would differ as it depends on the number of state transitions unique

for that choice.

* As the next state depends on input (choice) as well as current state we have designed a Mealy model.

Synthesis Report:

Release 12.1 - xst M.53d (nt)

Copyright (c) 1995-2010 Xilinx, Inc. All rights reserved.

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.45 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.47 secs

--> Reading design: VM1.prj

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6.1) Advanced HDL Synthesis Report

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8) Partition Report

9) Final Report

9.1) Device utilization summary

9.2) Partition Resource Summary

9.3) TIMING REPORT

=========================================================================

\* Synthesis Options Summary \*

=========================================================================

---- Source Parameters

Input File Name : "VM1.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "VM1"

Output Format : NGC

Target Device : xc3s200-5-pq208

---- Source Options

Top Module Name : VM1

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : lut

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : YES

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : YES

Resource Sharing : YES

Asynchronous To Synchronous : NO

Multiplier Style : auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 500

Add Generic Clock Buffer(BUFG) : 8

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Yes

Use Synchronous Set : Yes

Use Synchronous Reset : Yes

Pack IO Registers into IOBs : auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Library Search Order : VM1.lso

Keep Hierarchy : NO

Netlist Hierarchy : as\_optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=========================================================================

=========================================================================

\* HDL Compilation \*

=========================================================================

Compiling verilog file "VM1.v" in library work

Module <VM1> compiled

No errors in compilation

Analysis of file <"VM1.prj"> succeeded.

=========================================================================

\* Design Hierarchy Analysis \*

=========================================================================

Analyzing hierarchy for module <VM1> in library <work> with parameters.

a = "000"

b = "001"

c = "010"

d = "011"

op = "100"

=========================================================================

\* HDL Analysis \*

=========================================================================

Analyzing top module <VM1>.

a = 3'b000

b = 3'b001

c = 3'b010

d = 3'b011

op = 3'b100

Module <VM1> is correct for synthesis.

=========================================================================

\* HDL Synthesis \*

=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <VM1>.

Related source file is "VM1.v".

Found finite state machine <FSM\_0> for signal <state>.

-----------------------------------------------------------------------

| States | 5 |

| Transitions | 33 |

| Inputs | 8 |

| Outputs | 4 |

| Clock | clk (rising\_edge) |

| Reset | reset (positive) |

| Reset type | asynchronous |

| Reset State | 000 |

| Encoding | automatic |

| Implementation | LUT |

-----------------------------------------------------------------------

Summary:

inferred 1 Finite State Machine(s).

Unit <VM1> synthesized.

=========================================================================

HDL Synthesis Report

Found no macro

=========================================================================

=========================================================================

\* Advanced HDL Synthesis \*

=========================================================================

Analyzing FSM <FSM\_0> for best encoding.

Optimizing FSM <state/FSM> on signal <state[1:3]> with user encoding.

-------------------

State | Encoding

-------------------

000 | 000

100 | 100

010 | 010

011 | 011

001 | 001

-------------------

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# FSMs : 1

=========================================================================

=========================================================================

\* Low Level Synthesis \*

=========================================================================

Optimizing unit <VM1> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block VM1, actual ratio is 0.

Final Macro Processing ...

=========================================================================

Final Register Report

Macro Statistics

# Registers : 3

Flip-Flops : 3

=========================================================================

=========================================================================

\* Partition Report \*

=========================================================================

Partition Implementation Status

-------------------------------

No Partitions were found in this design.

-------------------------------

=========================================================================

\* Final Report \*

=========================================================================

Final Results

RTL Top Level Output File Name : VM1.ngr

Top Level Output File Name : VM1

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

Design Statistics

# IOs : 8

Cell Usage :

# BELS : 10

# LUT3 : 1

# LUT4 : 6

# LUT4\_L : 1

# MUXF5 : 1

# MUXF6 : 1

# FlipFlops/Latches : 3

# FDC : 3

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 7

# IBUF : 4

# OBUF : 3

=========================================================================

Device utilization summary:

---------------------------

Selected Device : 3s200pq208-5

Number of Slices: 4 out of 1920 0%

Number of Slice Flip Flops: 3 out of 3840 0%

Number of 4 input LUTs: 8 out of 3840 0%

Number of IOs: 8

Number of bonded IOBs: 8 out of 141 5%

Number of GCLKs: 1 out of 8 12%

---------------------------

Partition Resource Summary:

---------------------------

No Partitions were found in this design.

---------------------------

=========================================================================

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

------------------

-----------------------------------+------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

clk | BUFGP | 3 |

-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:

----------------------------------------

-----------------------------------+------------------------+-------+

Control Signal | Buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

reset | IBUF | 3 |

-----------------------------------+------------------------+-------+

Timing Summary:

---------------

Speed Grade: -5

Minimum period: 3.393ns (Maximum Frequency: 294.729MHz)

Minimum input arrival time before clock: 3.847ns

Maximum output required time after clock: 6.441ns

Maximum combinational path delay: No path found

Timing Detail:

--------------

All values displayed in nanoseconds (ns)

=========================================================================

Timing constraint: Default period analysis for Clock 'clk'

Clock period: 3.393ns (frequency: 294.729MHz)

Total number of paths / destination ports: 12 / 3

-------------------------------------------------------------------------

Delay: 3.393ns (Levels of Logic = 2)

Source: state\_FSM\_FFd3 (FF)

Destination: state\_FSM\_FFd3 (FF)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: state\_FSM\_FFd3 to state\_FSM\_FFd3

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 7 0.626 0.929 state\_FSM\_FFd3 (state\_FSM\_FFd3)

LUT4:I3->O 1 0.479 0.704 state\_FSM\_FFd3-In\_SW1 (N10)

LUT4:I3->O 1 0.479 0.000 state\_FSM\_FFd3-In (state\_FSM\_FFd3-In)

FDC:D 0.176 state\_FSM\_FFd3

----------------------------------------

Total 3.393ns (1.760ns logic, 1.633ns route)

(51.9% logic, 48.1% route)

=========================================================================

Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 18 / 3

-------------------------------------------------------------------------

Offset: 3.847ns (Levels of Logic = 3)

Source: choice<1> (PAD)

Destination: state\_FSM\_FFd1 (FF)

Destination Clock: clk rising

Data Path: choice<1> to state\_FSM\_FFd1

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 6 0.715 1.148 choice\_1\_IBUF (choice\_1\_IBUF)

LUT3:I0->O 1 0.479 0.851 state\_FSM\_FFd1-In11 (N01)

LUT4:I1->O 1 0.479 0.000 state\_FSM\_FFd1-In1 (state\_FSM\_FFd1-In)

FDC:D 0.176 state\_FSM\_FFd1

----------------------------------------

Total 3.847ns (1.849ns logic, 1.998ns route)

(48.1% logic, 51.9% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 3 / 3

-------------------------------------------------------------------------

Offset: 6.441ns (Levels of Logic = 1)

Source: state\_FSM\_FFd3 (FF)

Destination: y<0> (PAD)

Source Clock: clk rising

Data Path: state\_FSM\_FFd3 to y<0>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDC:C->Q 7 0.626 0.906 state\_FSM\_FFd3 (state\_FSM\_FFd3)

OBUF:I->O 4.909 y\_0\_OBUF (y<0>)

----------------------------------------

Total 6.441ns (5.535ns logic, 0.906ns route)

(85.9% logic, 14.1% route)

=========================================================================

Total REAL time to Xst completion: 7.00 secs

Total CPU time to Xst completion: 6.87 secs

-->

Total memory usage is 186232 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 0 ( 0 filtered)

Number of infos : 0 ( 0 filtered)